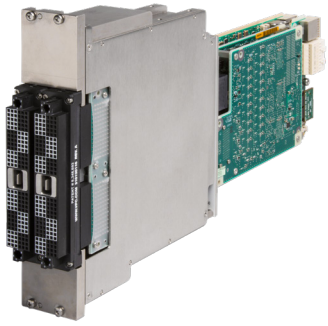
HSSub-9XXX Flexible IO Instrument

Reconfigurable PXI Express Instrument for a Wide Range of Serial Buses



Overview

Reconfigurable Flexible IO Expansion Instruments (FIOXI) address a wide range of requirements from legacy to special I/O bus capability backed by FPGA with powerful Test Defined FPGAs and tightly integrated memory for low level (tier 1) support. The 2-slot PXIe instrument combines a common reconfigurable Test Defined FPGA backbone with two bus-specific Physical Interface Modules (PIMs) that reduce or eliminate the need for external interface circuitry. Teradyne develops PIMs that are integrated in various combinations to provide physical I/O configurability. When Real-Time Computing (tier 2) is required, instruments are associated in software with any available HSSub RT Processor, otherwise they may be directly controlled by the HSSub Windows computer. Current PIM capabilities include RS485 (32 pairs), RS232 (up to 36 ports)/IRIG-B, HOTLink/ECL, and 1G Ethernet.

The FIOXI instruments include the following two PIM configurations:

- HSSub-9030 RS485/HOTLink/ECL FIOXI
- HSSub-9050 RS232/IRIG-B/Ethernet FIOXI
- HSSub-9080 RS485/RS232/IRIG-B FIOXI
- HSSub-9100 RS485 (64 pair) FIOXI
- HSSub-9110 RS232/IRIG-B/HOTLink/ECL FIOXI

The FIOXI instruments include the following single PIM configurations:

- HSSub-9010 RS485 (32 pair) FIOXI
- HSSub-9060 RS232/IRIG-B FIOXI
- HSSub-9070 HOTLink/ECL FIOXI

Features

- Two-slot PXIe instrument with flexible Physical Interface Module (PIM) architecture eliminate the need for external interface circuitry
- Large reconfigurable FPGA and memory supports multiple concurrently operating bus types
- TPS-configured in seconds by HSSub Apps

Benefits

- HSSub App configurability avoids the risk and cost obsolescence from new or changing requirements
- Capable and flexible programming minimizes TPS development and support costs
- High production throughput minimizes equipment and labor costs
- Long-term product and service support minimizes logistics and TPS support costs over the platform lifecycle

General Specifications	
PXI Characteristics	PXI Express (PCIe Gen 2 x4) 3U 2-slot
Test Defined FPGA (TDF)	Xilinx Virtex 7 XC7VX485T
Memory	1 GB DDR3 on Processor, 2 GB DDR3 memory on TDF 37 Mb Block RAM internal to Virtex 7 FPGA
Front Panel Connector	Samtec p/n HDI6-035-01RA
Instrument Triggers	Single ended & differential: (1) Input and (1) Output
Optional VPC Funnel	QuadraPaddle module (i2 MX cable and G20 ITA capability)
RS-485 I/O PIM Capability	
RS485 I/O Characteristics	32 Bidirectional differential pairs, half duplex, 50 Mbps max
Termination	120 ohms differential, selectable
HOTLink/ECL PIM Capability	
HOTLink I/O Characteristics	4 full duplex, 200 – 1500 Mb/s (Cypress CYP15G0401)
ECL I/O Characteristics	12 differential inputs, 12 differential outputs, 60 Mbps max
ECL Termination	TX: 280 ohms to -5.2V RX: 100 ohms
RS232/IRIG-B PIM I/O Capability	
RS232 PIM I/O	6 ports with full handshaking signals, 36 with none ½ of ports 1 Mbps/low voltage – ½ of ports 115 kbps/high voltage Emulates Data Terminal Equipment (DTE) or Data Computing Equipment (DCE)
IRIG-B Time Code Signals	1 PPS RS422 input and output IRIG-B Code RS422 input and output
IRIG-B Code Modulation	Amplitude, Manchester, or none
Ethernet PIM Capability	
Copper I/O Characteristics	8 concurrent channels (10/100/1000 Mb/s)
Optical I/O Characteristics	2 concurrent channels of Gigabit Ethernet 1000BASE-SX
Mixed Copper and Optical I/O	Concurrent operation of 6 copper and 2 optical channels

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