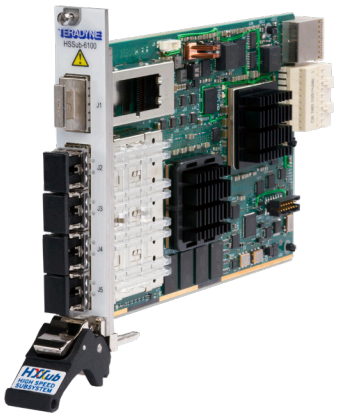
HSSub-6100 12G Serial I/O Instrument

Multiple Port Reconfigurable PXI Express Instrument for a Wide Range of Fast Serial Buses

The HSSub-6100 is a high-density, high-performance reconfigurable instrument supporting multiple concurrently operating high-speed serial buses that are typically optical. Pluggable SFP/SFP+/QSFP+ transceivers provide flexibility to support any I/O requirements. As a member of the Teradyne High Speed Subsystem (HSSubTM) family, this instrument benefits from the proven power and flexibility of the Three Tier Architecture and the ease of implementation provided by the TriFlexTM subsystem-wide infrastructure software. The HSSub-6100 is reconfigurable to address immediate and future requirements, and to avoid the high cost of obsolescence.



Background

The continuing trends in weapon system bus requirements include faster speed, higher bandwidth, and greater reliability. Defense and Aerospace assemblies now employ a variety of digital bus types and speeds such as Fibre Channel, Ethernet, Serial Rapid I/O, Serial FPDP, PCI Express, Xilinx Aurora, and Altera Serial Lite at speeds of 10Mb/s to 10Gb/s. These standardized buses are replacing the slower parallel and serial buses of the past. It is common for an assembly to employ multiple I/O ports and various bus types. As speeds increase to 1Gb/s and beyond, copper cabling is being displaced by fiber optics. Most often, application-level access is provided by Upper Level Protocols that simplify TPS development by hiding complex low-level bus details. The HSSub-6100 Reconfigurable 12G Serial Instrument is designed to directly address all of these ever-increasing demands.

HSSub Architecture

HSSub employs a Three Tier Architecture consisting of:

- Low-level I/O Protocol Processing
- Real-Time Computing
- WindowsTM-based Resource Management and TPS development

The HSSub TriFlex infrastructure software integrates all of the hardware. For a specific bus requirement, an HSSub App configures the hardware at each tier, and provides a conventional TPS programming interface on the Tier 3 Windows Computer.

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Features

- Up to 8 serial I/O ports to 12.5Gb/s
- Pluggable SFP/SFP+/QSFP+ transceivers for flexible optical and copper-based I/O capability
- Multiple concurrently operating buses
- Large, fast FPGA and memory provide high bandwidth and low latency
- TPS-configured in seconds by HSSub Apps

Benefits

- HSSub App architecture avoids the risk and cost obsolescence from new or changing requirements
- Capable and flexible programming minimizes TPS development and support costs
- High production throughput minimizes equipment and labor costs
- Long-term product and service support minimizes logistics and TPS support costs over the platform lifecycle

HSSub App configures the hardware at each tier, and provides a conventional TPS programming interface on the Tier 3 Windows Computer.

The HSSub-6100 instrument primarily addresses Tier 1, implementing the low-level bus protocol for standard, custom, legacy, and future bus requirements. Most standard bus types are addressed with readily available, proven FPGA code that is encapsulated in an HSSub App. The TPS developer then uses the HSSub App to rapidly configure the instruments and to access the functionality from Windows.

HSSub Tier 2 implements Upper Level Protocols such as video, data processing, or communications operations. Often these protocols are semi-standard or custom, and they may require fast and repeatable real-time performance. Some of this may be implemented in the HSSub-6100 FPGA, or passed to a Real-Time Processing Module or another FPGA-based instrument in the HSSub. If real-time performance is not required, the HSSub-6100 can interact directly with the Windows computer. All of this functionality is embedded in an HSSub App which is developed using totally open interfaces by Teradyne, third parties, or end users.

The HSSub-6100 has the capacity and speed to support multiple bus ports that are operating concurrently. The bus I/O is provided by SFP/SFP+/QSFP+ pluggable transceivers that can be selected to meet the precise requirements for speed, protocol, and optical characteristics. For certain buses, transceivers are available to provide copper-based I/O's as well.

Summary

The HSSub-6100 addresses the requirements for increasingly fast serial buses, mostly optical, that are common to virtually all new weapon system designs and many legacy platform upgrades. This instrument can be part of a complex integrated subsystem, or it can be used as an individual instrument. Designed and supported specifically for the Defense and Aerospace market, the HSSub-6100 can provide the core functionality for these serial bus requirements for decades to come.

Specifications	
PXI Characteristics	PXI Express (PCIe Gen 2 x8) 3U 1-slot
Front Panel Connectors	• (4) SFP+ transceiver connectors • (1) QSFP+ transceiver connector • All QSFP+/SFP+ transceivers connect directly to the Test Defined FPGA Xilinx GTX transceivers
Test Defined FPGA	Xilinx Kintex UltraScale KU035
Memory	4GB of DDR4 memory controlled by Test Defined FPGA
Maximum I/O Speed per Front Panel SFP+	12.5 Gb/s
Maximum I/O Speed per Front Panel QSFP+	12.5 Gb/s per lane (4 lanes) (Note: QSFP+ transceivers not supplied)
Maximum Backplane Bandwidth	>1.25 GB/s
Bit Error Rate Test (BERT)	Teradyne BERT HSSub App is included. BERT can test Fixtures with loopback capabilities or UUTs with PRBS capabilities
SFP+ Transceivers	Includes 4 SFP+ optical transceivers supporting multiple protocols with data rates from 1-10 Gb/s

Part Numbers	
634-540-80	HSSub-6100 12G Serial I/O Expansion Instrument
710-059-03	Spare SFP+ Optical Transceiver (optional)

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